In the Claims:

1-19. (cancelled)

20. (new) A synchronous dynamic random access memory device comprising:

A. a single chip integrated circuit;

B. a dynamic random access memory array formed on the chip, the array including plural array data leads carrying parallel data signals to the array and parallel array address leads carrying parallel address signals to the array, one data signal representing one data bit and one address signal representing one address bit, the array being organized in plural addressable locations with each location being randomly addressable by the address signals for writing one word of data bits from the array data leads to each addressed location;

C. a clock signal terminal formed on the chip for receiving a clock signal formed of rising and falling edges regularly spaced in time, the clock signal being continuous during operation of the device;

D. plural address terminals formed on the chip and receiving parallel address signals from external the chip, the received address signals occurring in plural groups separated in time, a first group of address signals being received at a first time and a second group of address signals being received at a second time after the first time, the address signals being received at the same time as the clock terminal receives the continuous clock signal, the received address signals indicating an address of a random location in the array;

E. plural address registers formed on the chip and having address inputs coupled to the plural address terminals, the address registers including a first address register having a first control input lead receiving a first

control input signal for latching the first group of address signals, and a second address register having a second control input lead receiving a second control signal for latching the second group of address signals, the first and second address registers each having register address output leads;

F. an address multiplexer formed on the chip, the address multiplexer having a first set of address inputs, a second set of address inputs, and multiplexer address output leads, the first set of address inputs being coupled to the plural address terminals and receiving the first and second groups of address signals, each input of the second set of address inputs receiving alternate address signals, the address multiplexer having a select signal input to select either the first set of inputs or the second set of inputs to be output at the multiplexer address output leads;

G. an address sequencer formed on the chip, the address sequencer having a clock signal input lead coupled to the clock signal terminal, address input leads coupled to the plural address terminals by a series connection of the address multiplexer and the plural address registers, and array address output leads coupled to the array address leads, the address sequencer receiving the address signals from the address terminals and providing a sequence of address signals to the array address leads to access addressable locations in the array, starting from the address received from the address terminals, synchronous with the clock;

H. a control strobe terminal formed on the chip and receiving a control strobe signal at the same time as the clock signal terminal receives the clock signal and at the same time as the address terminals receive the parallel address signals;

I. a command decoder formed on the chip and having a plurality of control inputs, a first control output coupled to the first control input lead, and a second control output coupled to the second control input lead, one of the control inputs of the command decoder being coupled to the control strobe terminal and receiving the control strobe signal, the command decoder generating a first control signal on the first control output in response to the control strobe signal and a first set of control signals received on the control inputs, and generating a second control signal on the second control output in response to the control strobe signal and a second set of control signals received on the control inputs; and

J. a data port formed on the chip and connecting with the array data leads and the clock signal terminal, the data port including:

i. plural data terminals for receiving parallel data signals synchronous with the clock, each set of parallel data signals representing one data word; and

ii. at least a write serial latch serially connected between the data terminals and the array data leads, the at least a write serial latch serially latching the data word signals received at the data terminals synchronous with the clock signal and carrying the received data signals to the array data leads for writing the data signals in the array at the random location indicated by the received address signals.

21. (new) The device of claim 20 in which the first set of address inputs of the address multiplexer are coupled to the register address output leads of the plural address

registers, and the address output leads of the address multiplexer are coupled to the address input leads of the address sequencer.

22. (new) The device of claim 20 including a latch circuit formed on the chip, the latch circuit having an input coupled to a third control output of the command decoder and having a select output connected to the select signal input of the address multiplexer.

23. (new) The device of claim 22 in which the latch circuit includes a clear input coupled to a fourth control output of the command decoder.

24. (new) The device of claim 20 in which the plural registers of the address port include an address buffer register that includes the first and second address registers, the plural registers of the address port include an alternate address buffer register, and the address input leads of the address sequencer are selectively coupled to the register address output leads of the address buffer register and the alternate address buffer register by the address multiplexer.

25. (new) The device of claim 20 in which at least some of the plurality of control inputs of the command decoder are coupled to the address terminals.

26. (new) The device of claim 20 in which all of the plurality of control inputs of the command decoder are coupled to the address terminals.

27. (new) A synchronous dynamic random access memory device comprising:

A. a single chip integrated circuit;

B. a dynamic random access memory array formed on the chip, the array including plural array data leads carrying parallel data signals to the array and parallel array address leads carrying parallel address signals to the array, one data signal representing one data bit and one address signal representing one address bit, the array being organized in plural addressable locations with each location being randomly addressable by the address signals for writing one word of data bits from the array data leads to each addressed location;

C. a clock signal terminal formed on the chip for receiving a clock signal formed of rising and falling edges regularly spaced in time, the clock signal being continuous during operation of the device;

D. plural address terminals formed on the chip and receiving parallel address signals from external the chip, the received address signals occurring in plural groups separated in time, a first group of address signals being received at a first time and a second group of address signals being received at a second time after the first time, the address signals being received at the same time as the clock terminal receives the continuous clock signal, the received address signals indicating an address of a random location in the array;

E. plural address registers formed on the chip and having address inputs coupled to the plural address terminals, the address registers including a first address register having a first control input lead receiving a first

control input signal for latching the first group of address signals, and a second address register having a second control input lead receiving a second control signal for latching the second group of address signals, the first and second address registers each having register address output leads;

F. an address multiplexer formed on the chip, the address multiplexer having a first set of address inputs, a second set of address inputs, and multiplexer address output leads, the first set of address inputs being coupled to the plural address terminals and receiving the first and second groups of address signals, each input of the second set of address inputs receiving alternate address signals, the address multiplexer having a select signal input to select either the first set of inputs or the second set of inputs to be output at the multiplexer address output leads;

G. an address sequencer formed on the chip, the address sequencer having a clock signal input lead coupled to the clock signal terminal, address input leads coupled to the address output leads of the address multiplexer, and array address output leads coupled to the array address leads, the address sequencer receiving the address signals from the address output leads of the address multiplexer and providing a sequence of address signals to the array address leads to access addressable locations in the array, starting from the address received from the address multiplexer, synchronous with the clock;

H. a control strobe terminal formed on the chip and receiving a control strobe signal at the same time as the clock signal terminal receives the clock signal and at the same time as the address terminals receive the parallel address signals;

I. a command decoder formed on the chip and having a plurality of control inputs, a first control output coupled to the first control input lead, and a second control output coupled to the second control input lead, one of the control inputs of the command decoder being coupled to the control strobe terminal and receiving the control strobe signal, the command decoder generating a first control signal on the first control output in response to the control strobe signal and a first set of control signals received on the control inputs, and generating a second control signal on the second control output in response to the control strobe signal and a second set of control signals received on the control inputs; and

J. a data port formed on the chip and connecting with the array data leads and the clock signal terminal, the data port including:

i. plural data terminals for receiving parallel data signals synchronous with the clock, each set of parallel data signals representing one data word;

ii. a first write serial latch having an input coupled to the the data terminals, the first write serial latch serially latching the data word signals received at the data terminals synchronous with the clock signal, the first write serial latch having an output; and

iii. a second write latch serially connected between the output of the first write serial latch and the array data leads, and carrying the data signals received from the first write serial latch to the array data leads for writing the data signals in the array at the random location indicated by the received address signals.

28. (new) The device of claim 27 in which the first set of address inputs of the address multiplexer are coupled to the register address output leads of the plural address registers, and the address output leads of the address multiplexer are coupled to the address input leads of the address sequencer.

29. (new) The device of claim 27 including a latch circuit formed on the chip, the latch circuit having an input coupled to a third control output of the command decoder and having a select output connected to the select signal input of the address multiplexer.

30. (new) The device of claim 29 in which the latch circuit includes a clear input coupled to a fourth control output of the command decoder.

31. (new) The device of claim 27 in which the plural registers of the address port include an address buffer register that includes the first and second address registers, the plural registers of the address port include an alternate address buffer register, and the address input leads of the address sequencer are selectively coupled to the register address output leads of the address buffer register and the alternate address buffer register by the address multiplexer.

32. (new) The device of claim 27 in which at least some of the plurality of control inputs of the command decoder are coupled to the address terminals.

33. (new) The device of claim 27 in which all of the plurality of control inputs of the command decoder are coupled to the address terminals.